

WHAT IS CLAIMED IS:

1 1. A transistor for an integrated circuit,
2 comprising:
3 a source region in a substrate;
4 a drain region in the substrate;
5 a channel region between the source and drain
6 regions, wherein the source and drain regions are separated by
7 a channel length; and
8 a plurality of pocket implants extending into the
9 channel region between the source region and the drain region
10 to cause a reverse short channel effect for the transistor.

1 2. The transistor of claim 1, wherein the
2 plurality of pocket implants merge in the channel region.

1 3. The transistor of claim 1, wherein the
2 plurality of pocket implants merge at a midpoint in the
3 channel length in the channel region.

1 4. The transistor of claim 1, wherein the pocket
2 implants are doped with a dopant of opposite polarity from
3 that used for the source and drain regions.

1 5. The transistor of claim 4, wherein the source
2 and drain regions are n-type, and the pocket implants are p-
3 type.

1 6. The transistor of claim 5, wherein the p-type
2 pocket implants are formed with a boron dopant.

1 7. The transistor of claim 6, wherein the pocket
2 implants are further doped with a blanket boron implant.

1 8. The transistor of claim 7, wherein a dosage of
2 the blanket boron implant is about 10^{11} cm⁻².

00606252 062800

9. The transistor of claim 4, wherein the source and drain regions are a p-type material, and the pocket implants are an n-type material.

10. The transistor of claim 9, wherein the n-type pocket implants are formed with a phosphorus dopant.

11. The transistor of claim 1, wherein due to the reverse short channel effect, the transistor has a higher punch-through voltage.

12. The transistor of claim 1, wherein the transistor is a native transistor.

13. The transistor of claim 12 where in an enhancement implant is absent from the channel region.

14. The transistor of claim 1 wherein the transistor has a channel length about equal to a channel length of a logic transistor in the same substrate.

15. The transistor of claim 1 wherein the pocket implants are formed by implantation at an angle.

16. A circuit in an integrated circuit, comprising:
first and second transistors coupled in series, each of the transistors comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region between the source and drain regions, wherein the source and drain regions are separated by a channel length; and

a plurality of pocket implants extending into the channel region between the source region and the drain region to cause a reverse short channel effect for the transistor.

091606252 062800

18. The circuit of claim 16, further comprising a capacitor in series with the first and second transistor.

19. The circuit of claim 18, wherein the circuit is a voltage pump.

20. The circuit of claim 16, wherein the circuit is ~~a memory cell.~~

21. A method of fabricating an integrated circuit comprising the steps of:
depositing a field implant;
depositing a well implant; and
depositing an enhancement implant, wherein the steps of depositing a field implant, depositing a well implant, and depositing an enhancement implant are done using a single mask.

22. The method of claim 21 wherein the well implant is an n-well implant.

23. The method of claim 21 wherein the well implant is a p-well implant.

24. The method of claim 21 further comprising the steps of:

- forming a high voltage native transistor by blocking the well implant and the enhancement implant; and
- offsetting the field implant from an active area of the native transistor, thereby obtaining high gated-diode junction breakdown characteristics.

only
194

1 26. The method of claim 21 further comprising the
2 step of:
3 depositing two pocket implants; and
4 merging the pocket implants together by lateral
5 diffusion, whereby a channel doping profile from the pocket
6 implant diffusion exhibits reverse-short-channel effect.

add
a.5

add 7

Add 7

ADD D4